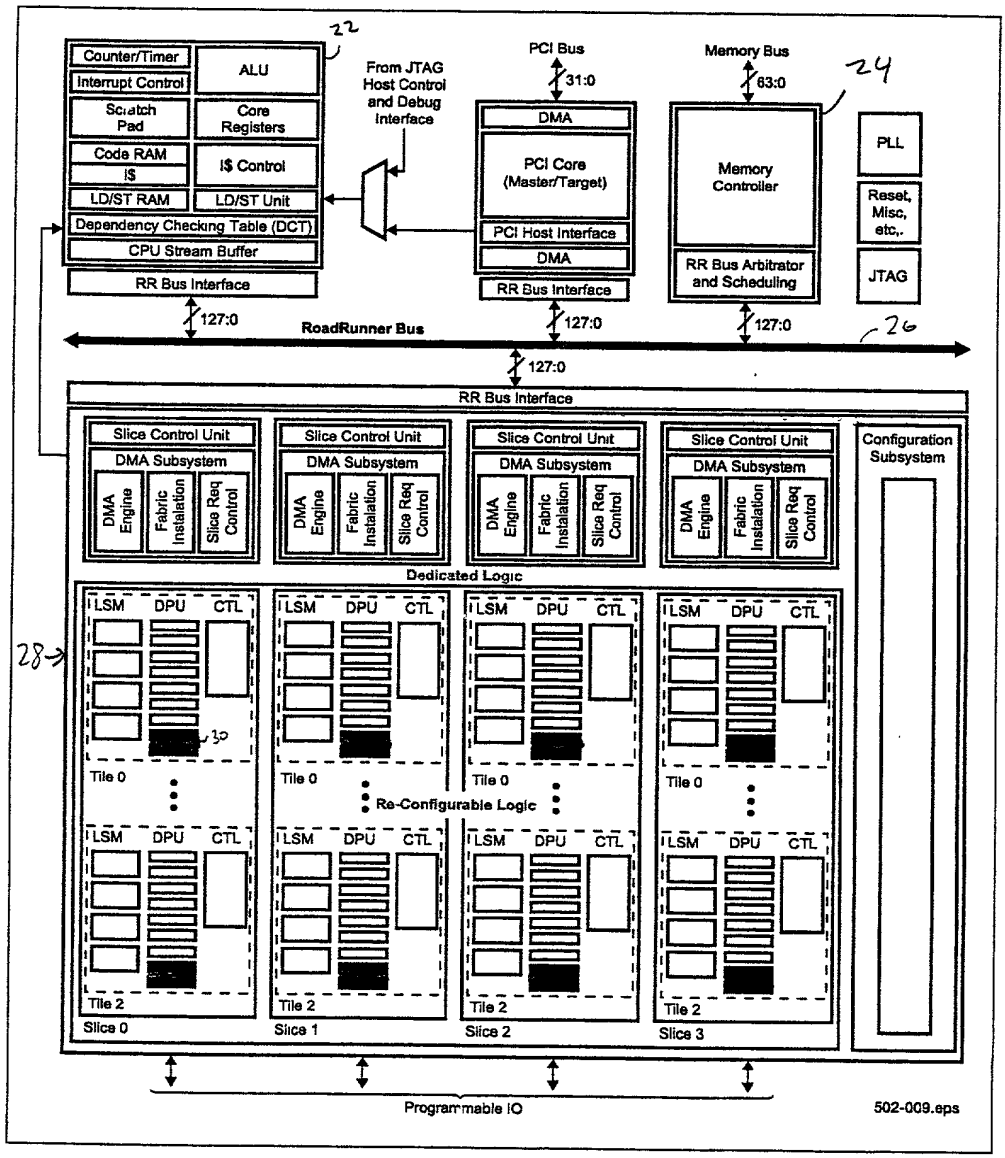

20
22
Counter/Timer
ALU
Interrupt Control
Scratch Pad
Core Registers
Code RAM
I$
I$ Control
LD/ST RAM
LD/ST Unit
Dependency Checking Table (DCT)
CPU Stream Buffer
RR Bus Interface
From JTAG Host Control and Debug Interface
PCI Bus
31:0
DMA
PCI Core (Master/Target)
PCI Host Interface
DMA
RR Bus Interface
Memory Bus
63:0
24
Memory Controller
RR Bus Arbitrator and Scheduling
PLL
Reset, Misc, etc,.
JTAG
127:0
RoadRunner Bus
127:0
127:0
26
127:0
RR Bus Interface
Slice Control Unit
DMA Subsystem
DMA Engine
Fabric Instalation
Slice Req Control
Configuration Subsystem
Dedicated Logic
28
LSM
DPU
CTL
30
Tile 0
Re-Configurable Logic
Tile 2
Slice 0
Slice 1
Slice 2
Slice 3
Programmable IO
502-009.eps

FIGURE 1

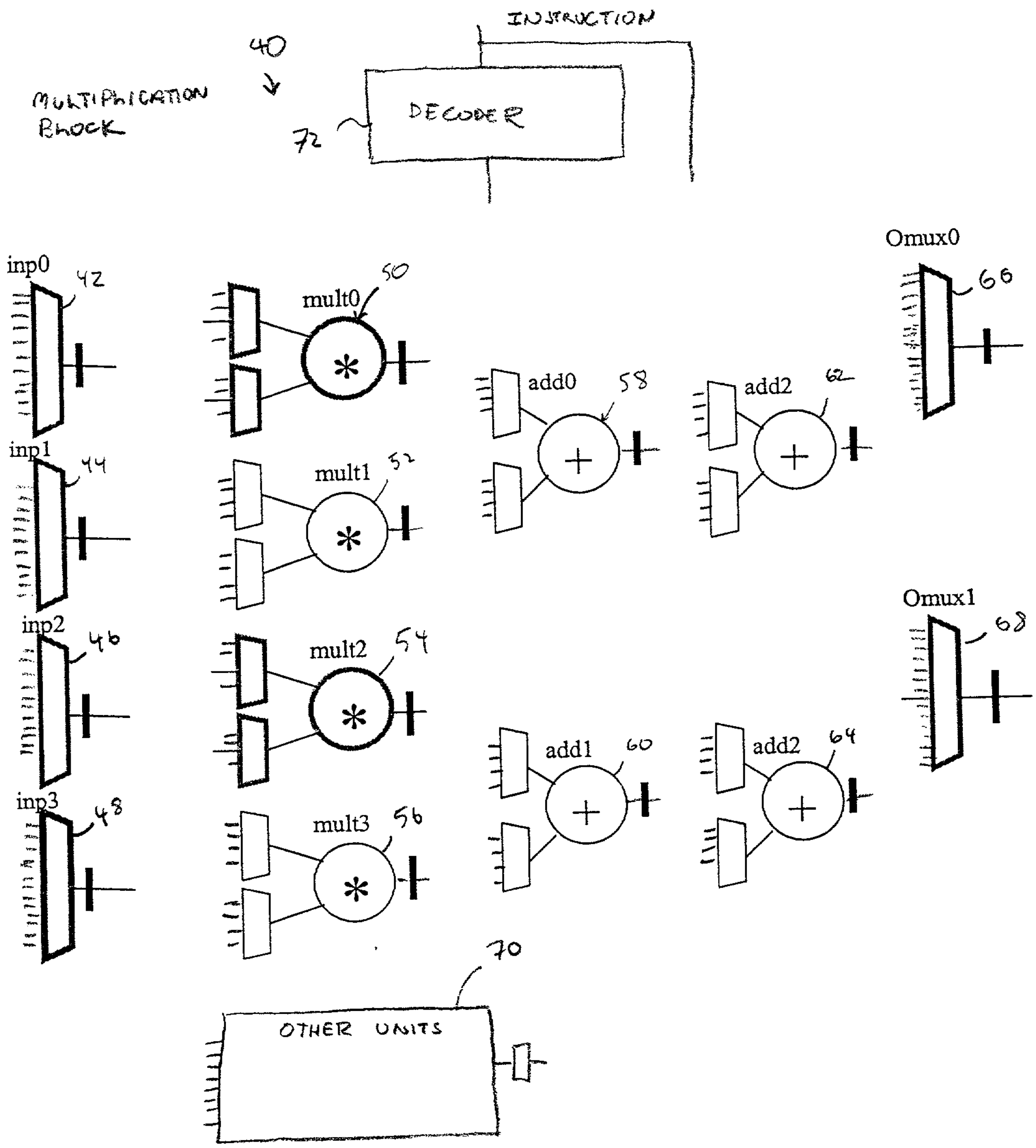
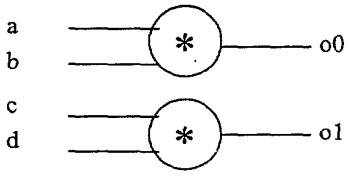

INSTRUCTION
40
MULTIPLICATION BLOCK
DECODER
72
inp0
42
inp1
44
inp2
46
inp3
48
mult0
50
mult1
52
mult2
54
mult3
56
add0
58
add1
60
add2
62
add2
64
Omux0
66
Omux1
68
OTHER UNITS
70

FIGURE 2

2MULT – CS2112 Compatible mode 2 independent multipliers



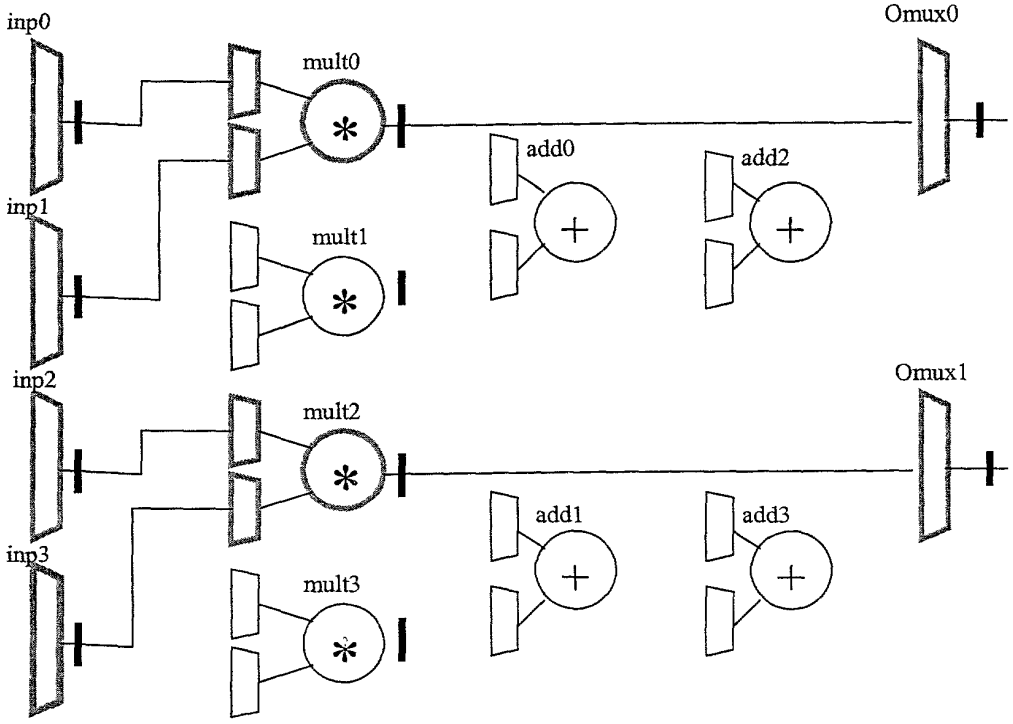
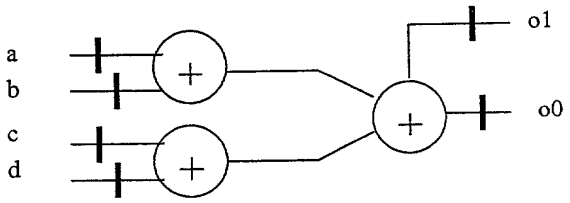


FIGURE 3A

4ADD32 – Sum of 4 32-bit inputs



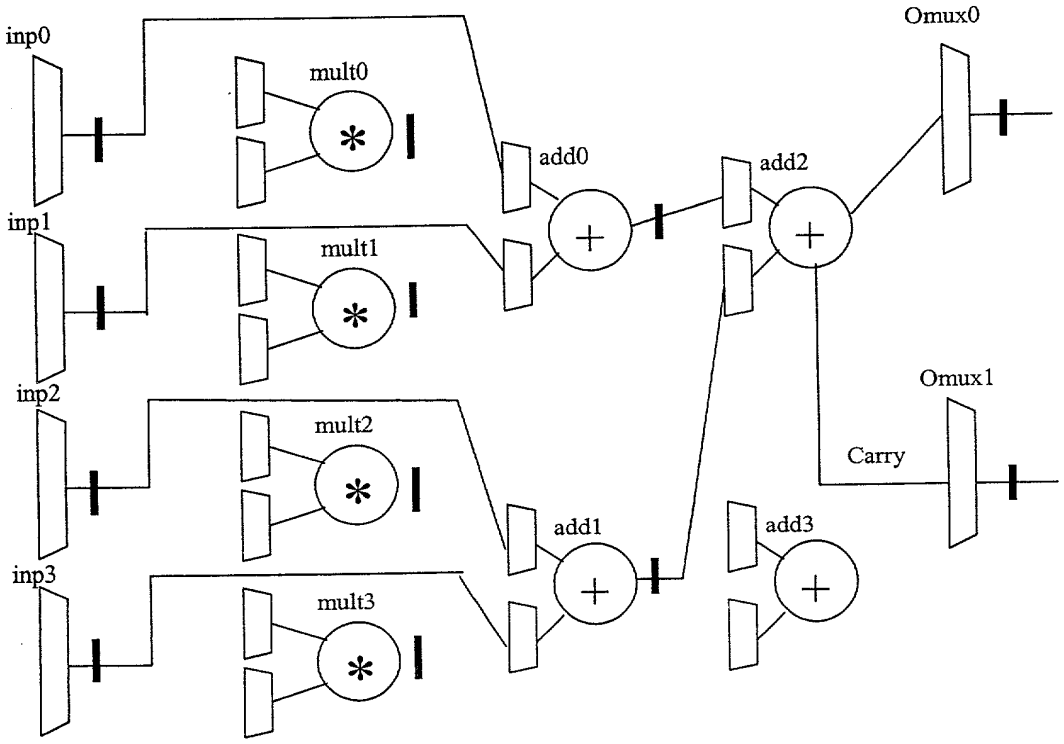
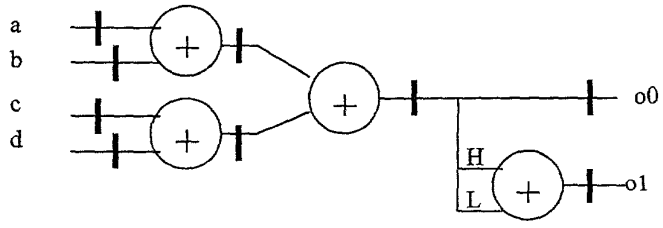


FIGURE 3B

4ADD16 – Sum of 4 packed 16-bit inputs, sum of upper, lower 16-bits



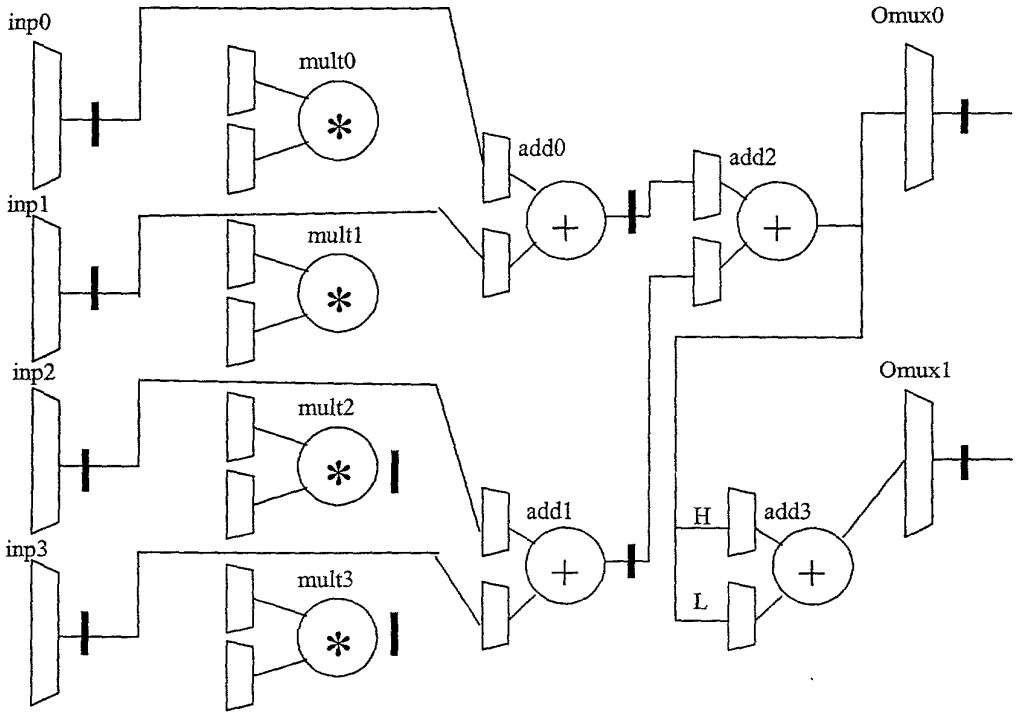
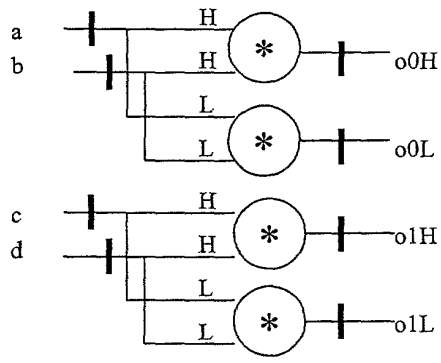


FIGURE 3C

4MULT – 4 multipliers with pack 16-bit inputs



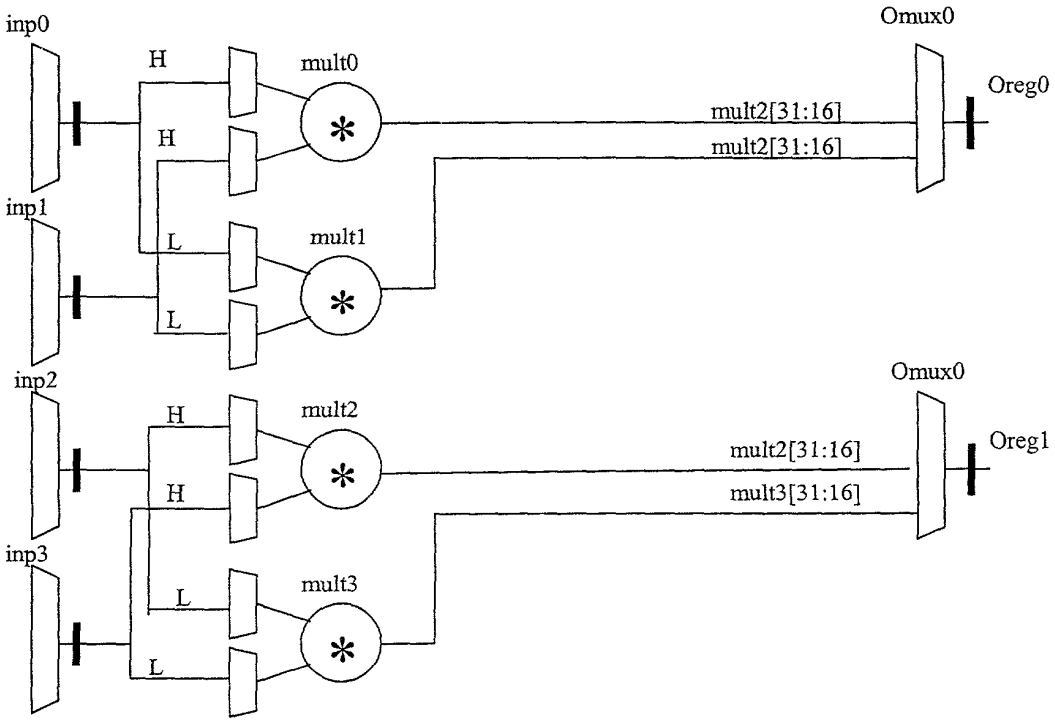
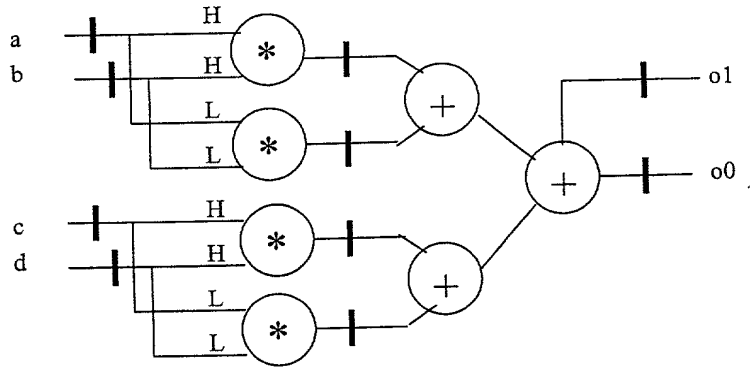


FIGURE 3D

4MULTSUM – Sum of 4 multipliers



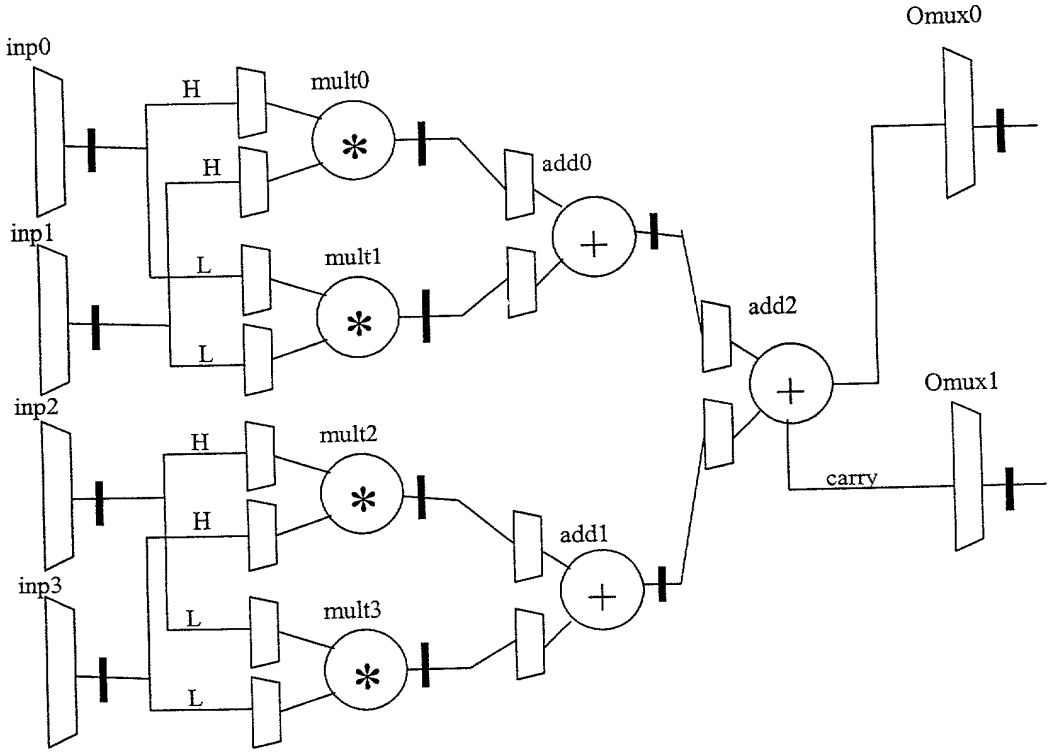
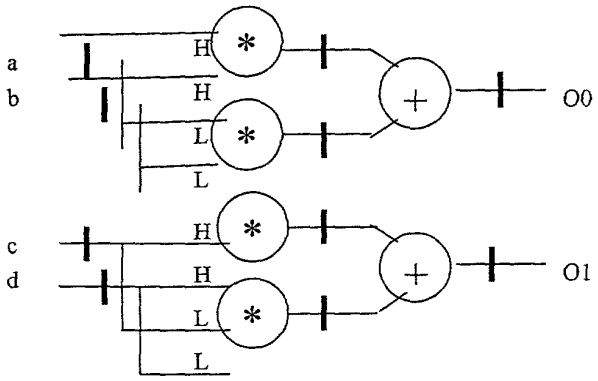


FIGURE 3E

4MULT2SUM – 2 Sums of 2 multipliers



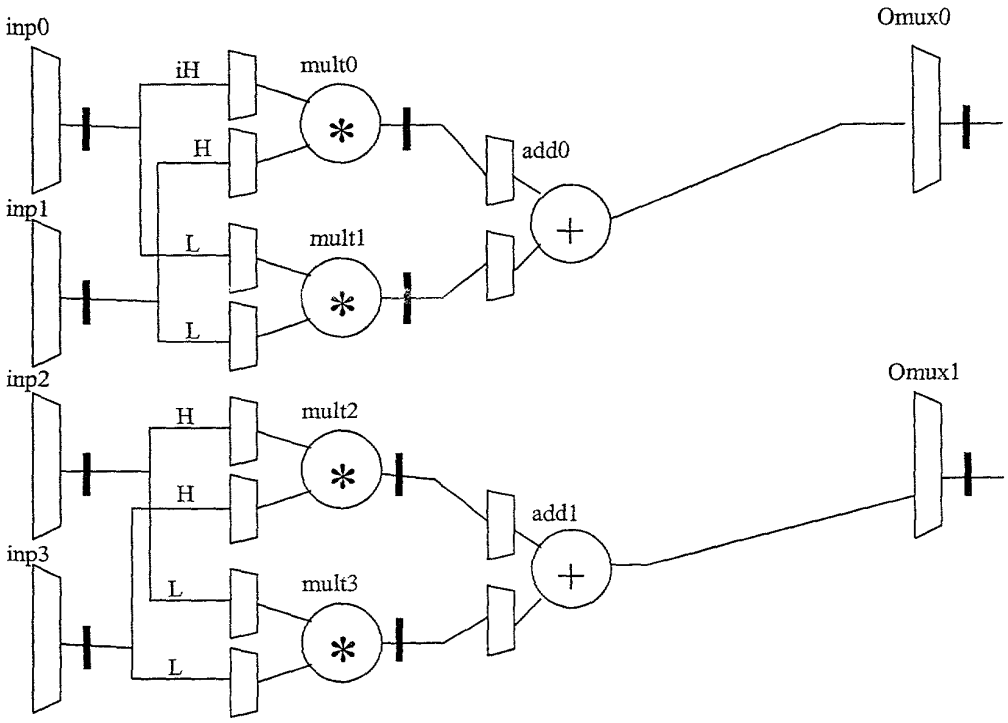
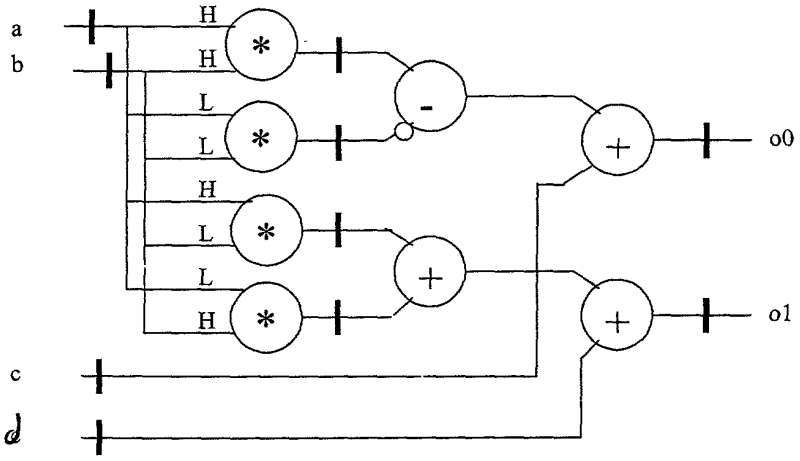


FIGURE 3F

CMULT – 32-bit output complex multiply with 32-Bit accumulation input, Assumes real part in High 16-bits, imaginary in Low 16-bits



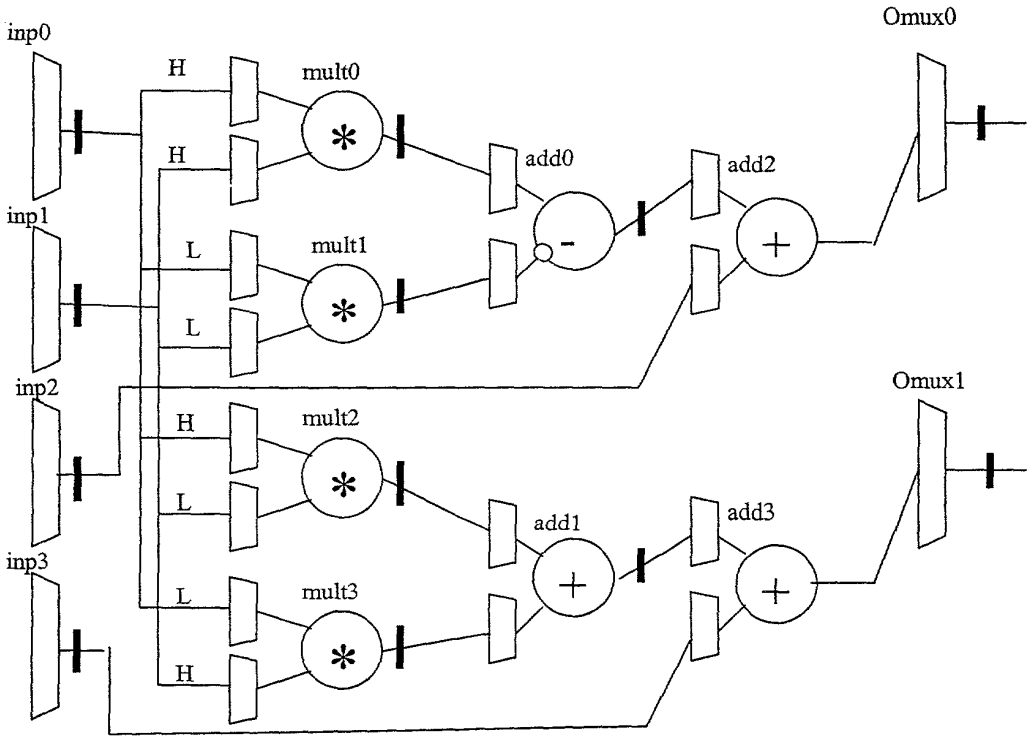
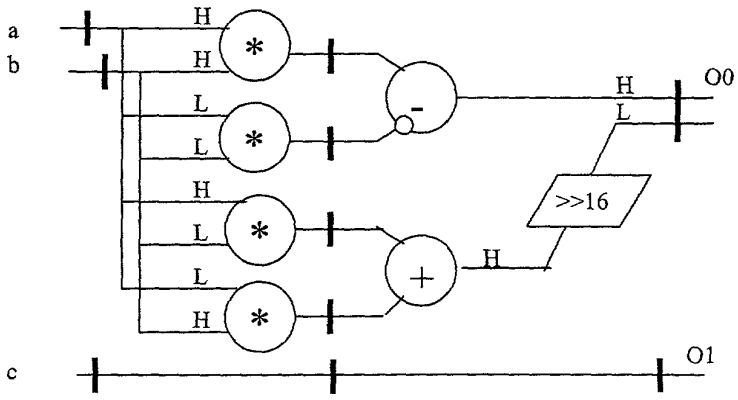


FIGURE 36

CMULT16 – Complex Multiplier with 16-Bit Packed data, and indepent delay path. Assumes real part in High 16-bits, imaginary in Low 16-bits



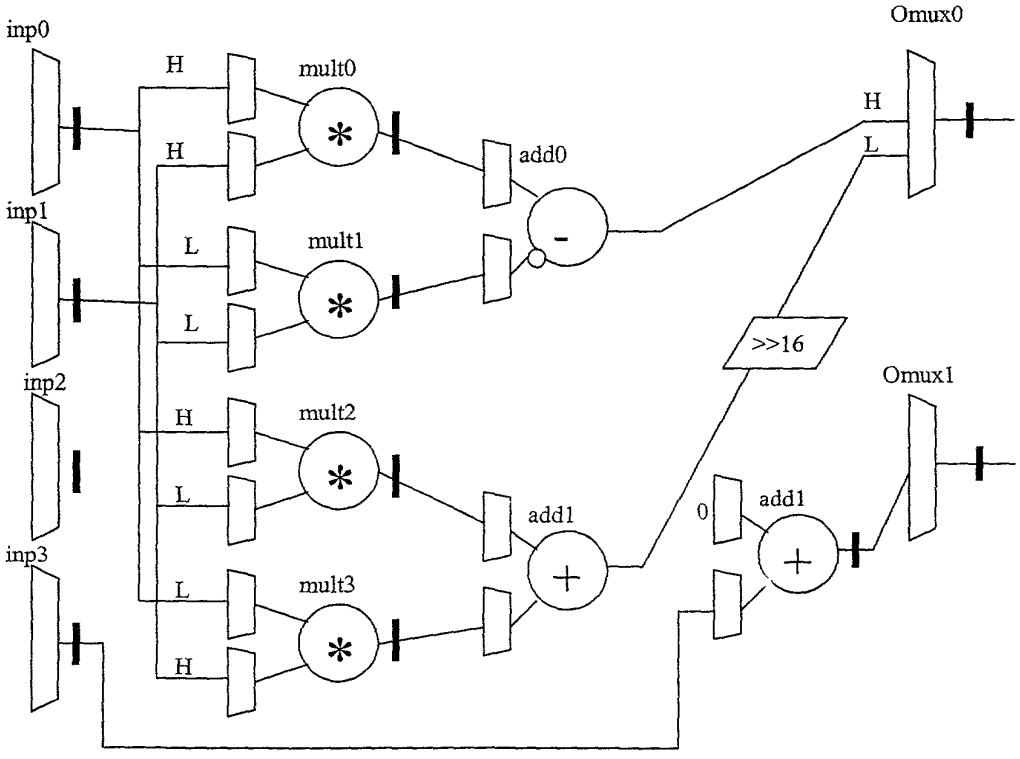
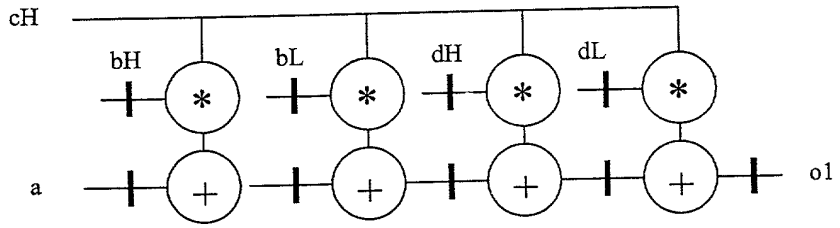


FIGURE 3H

4FIR - 4 tap FIR filter



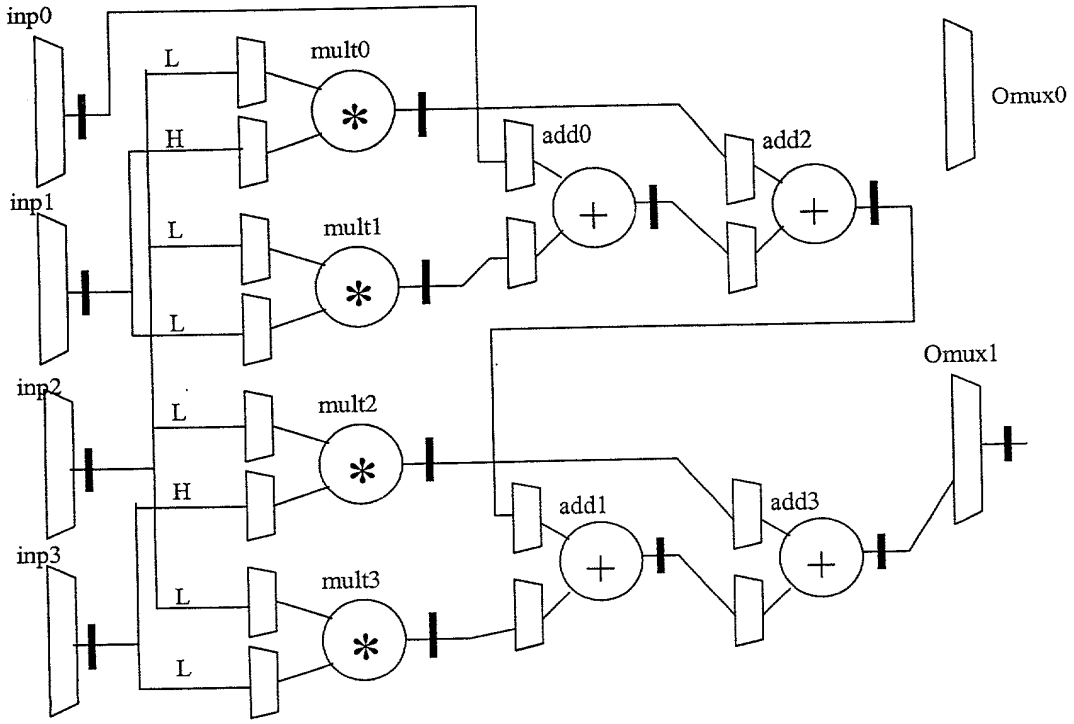


FIGURE 3I

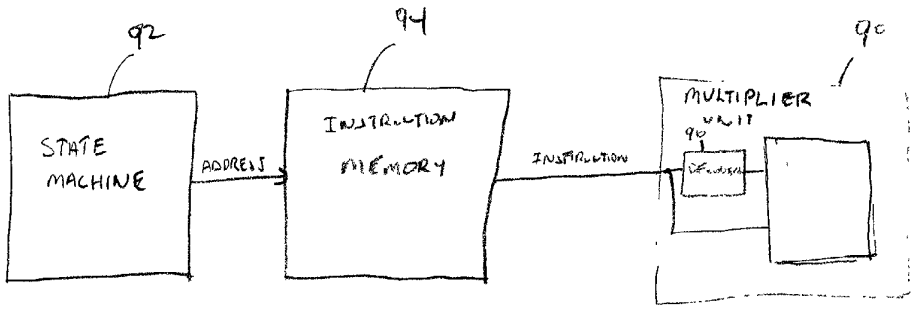


FIGURE 5

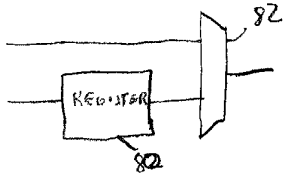


FIGURE 4

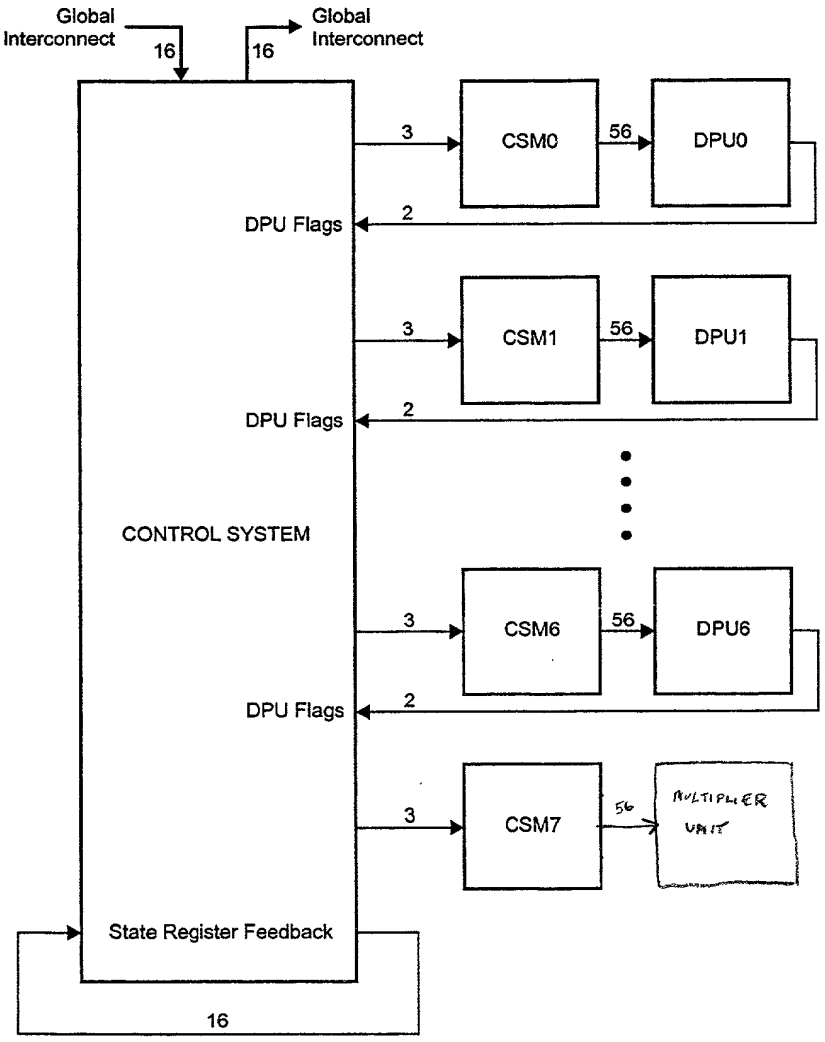

Global Interconnect
16
Global Interconnect
16
3
CSM0
56
DPU0
DPU Flags
2
3
CSM1
56
DPU1
DPU Flags
2
CONTROL SYSTEM
3
CSM6
56
DPU6
DPU Flags
2
3
CSM7
56
MULTIPLIER UNIT
State Register Feedback
16

FIGURE 6

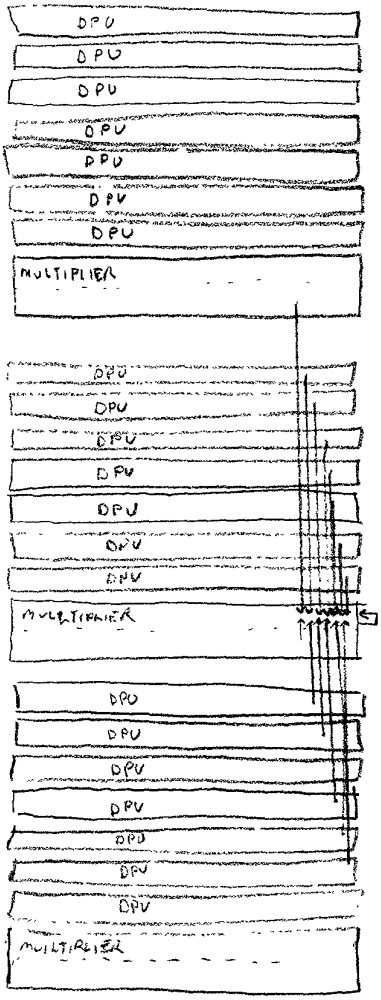

DPU
DPU
DPU
DPU
DPU
DPU
DPU
DPU
MULTIPLIER
DPU
DPU
DPU
DPU
DPU
DPU
DPU
MULTIPLIER
DPU
DPU
DPU
DPU
DPU
DPU
DPU
MULTIPLIER

FIGURE 7

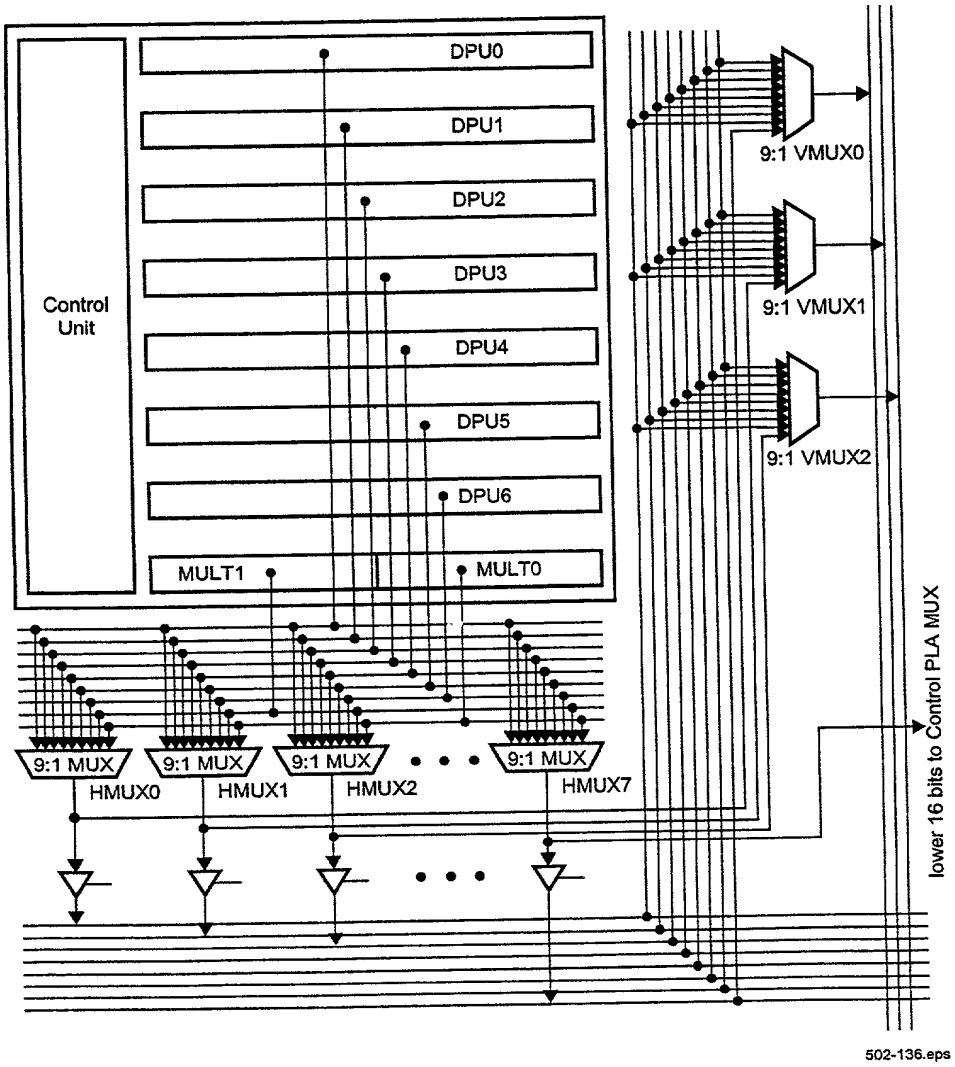

Control Unit
DPU0
DPU1
DPU2
DPU3
DPU4
DPU5
DPU6
MULT1
MULT0
9:1 VMUX0
9:1 VMUX1
9:1 VMUX2
9:1 MUX
9:1 MUX
9:1 MUX
9:1 MUX
HMUX0
HMUX1
HMUX2
HMUX7
lower 16 bits to Control PLA MUX
502-136.eps

FIGURE 8

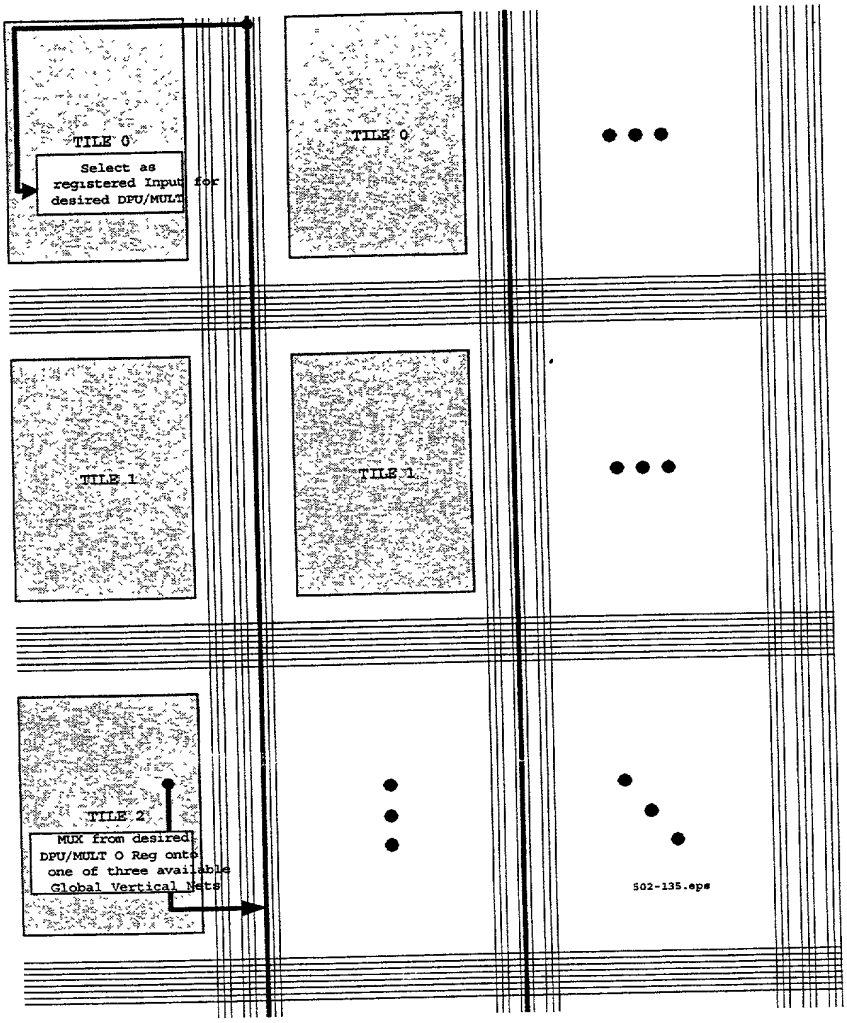

TILE 0
Select as registered Input for desired DPU/MULT
TILE 0
TILE 1
TILE 1
TILE 2
MUX from desired DPU/MULT O Reg onto one of three available Global Vertical Nets
502-135.eps

FIGURE 9

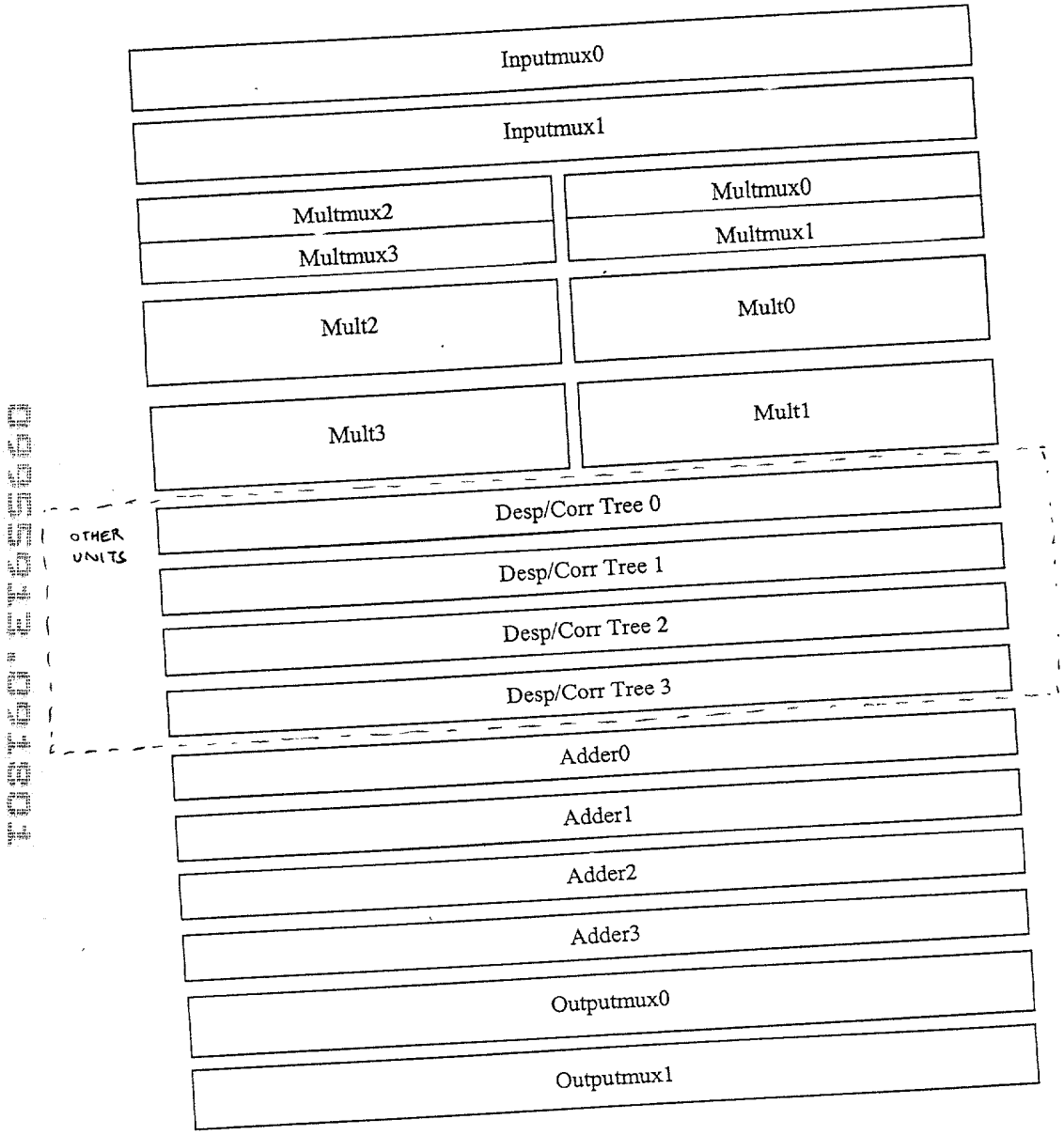

Inputmux0
Inputmux1
Multmux2
Multmux3
Multmux0
Multmux1
Mult2
Mult0
Mult3
Mult1
Desp/Corr Tree 0
Desp/Corr Tree 1
Desp/Corr Tree 2
Desp/Corr Tree 3
OTHER UNITS
Adder0
Adder1
Adder2
Adder3
Outputmux0
Outputmux1

FIGURE 10

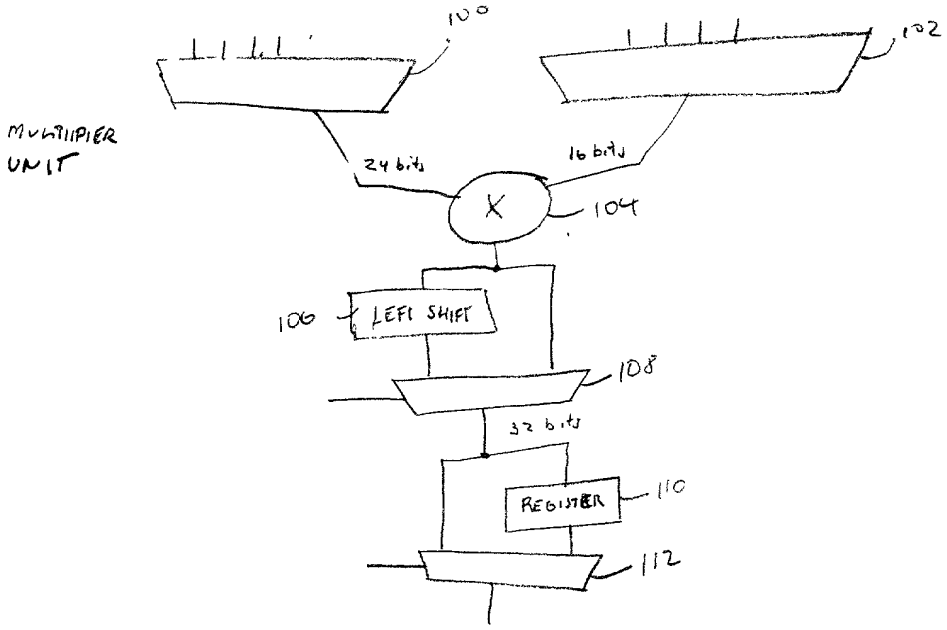


FIGURE 11

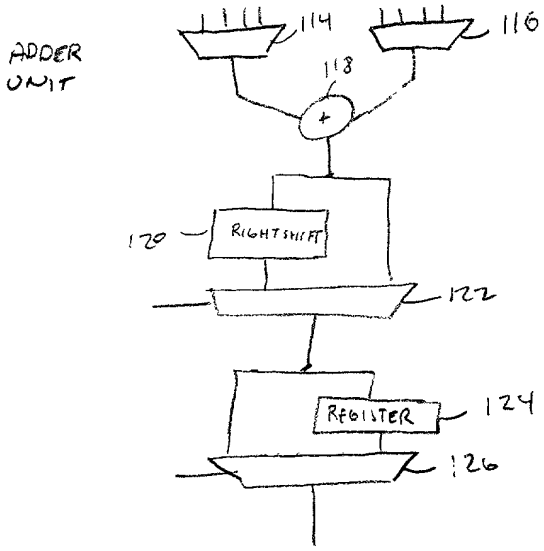


FIGURE 12

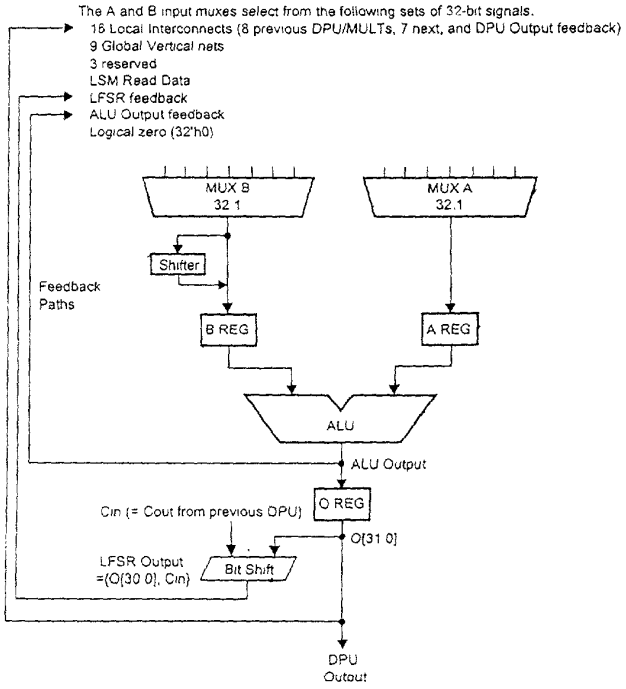

The A and B input muxes select from the following sets of 32-bit signals.
16 Local Interconnects (8 previous DPU/MULTs, 7 next, and DPU Output feedback)
9 Global Vertical nets
3 reserved
LSM Read Data
LFSR feedback
ALU Output feedback
Logical zero (32'h0)
MUX B
32:1
MUX A
32:1
Shifter
Feedback
Paths
B REG
A REG
ALU
ALU Output
O REG
Cin (= Cout from previous DPU)
O[31:0]
LFSR Output
={O[30:0], Cin}
Bit Shift
DPU
Output

FIGURE 13